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A REUNERT COMPANY

VF330

IO Processor card with Intel Cyclone® V FPGA for SWaP applications

OpenVPX
FMC™

SPECIFICATIONS

Cyclone® V GX Field Programmable Gate Array (FPGA) family

- High-performance FPGA fabric
- Internal memory blocks with soft error correction (ECC)
- Embedded variable-precision digital signal processing (DSP) blocks
- Native support for 9x9, 18x18 and 27x27 multipliers
- Embedded DDR3 memory controller with ECC support
- Low-power, high-speed serial transceivers up to 6.144 Gbps
- Two banks of up to 1GB external DDR3 memory per bank
- Tamper protection and AES design security features
- Optional single event upset (SEU) support

FPGA Mezzanine card (FMC) Interface

- LVDS signalling levels
- VITA 57 high pin count (HPC) FMC interface
- 4x HSSI lanes from FPGA
- LVDS / LVTTL interface on LA & HA
- Optional FMC IO connector

VPX Interface

- Various OpenVPX slot profiles, SLT3-PAY-1F2U-14.2.12 maximum envelope
- Data plane : One x4 Fat Pipe (PCIe Gen 1, Gen 2 and SRIO)
- Control Plane : Optional Ethernet TP (with magnetics) / UTP (without) build option
- Management PI. : Tier 1 IPMC support as per VITA 46.11
- Debug : 1x serial port and 1x FPGA USB Blaster
- FMC IO : 44x Differential pairs from FMC IO connector to P1 & P2

Software and Firmware Support

- Board Support Package (BSP)
  - Linux and Windows FPGA PCIe drivers
- FPGA firmware reference design
  - Example software for the VF360 & VF370 SBC processing cards
- MIL-STD-1553 firmware reference design and example software

Companion Modules

- VF360 SBC with Intel Stratix® V FPGA and C667x Ti KeyStone multicore DSP
- VF370 SBC with Intel Atom E39xx processor and Intel Cyclone® V FPGA
- FM501 Development FMC card
- VR301 Development Rear Transition Module (RTM)
- FM510 Video & IO FMC, FM560/565 Mil-IO / General IO FMC
- VT330 VPX Development Rack with 3-slot backplane, ATX power supply and fan

The **VF330** is a 3U OpenVPX IO Processor card that utilises Intel Cyclone® V FPGA technology and a FMC mezzanine site, to provide a module with scalable processing power and flexible IO options for reduced Size, Weight and Power (SWaP) applications. It is available in standard air-cooled and rugged conduction-cooled versions.

The combination of the Cyclone® V FPGA and the VITA 57 FMC site provides a highly flexible architecture that accommodates a wide range of processing and IO requirements by using IP cores and/or custom user logic inside the FPGA.

The Cyclone® V FPGA's high-performance fabric, internal memory, variable precision DSP blocks and high-speed serial interfaces (HSSI) facilitates high-bandwidth data transfer from the FMC, through the FPGA to the VPX backplane (or visa versa), with real-time processing inside the FPGA.

The two banks of external DDR3 memory connected to the FPGA supports algorithms with large memory size and bandwidth requirements.

The high pin count (HPC) FMC connector connects to the FPGA through a high-speed serial interface (HSSI) and LVDS/LVTTL signals. The optional FMC IO connector routes 44 differential signals to the P1 & P2 VPX connectors for backplane- or rear-IO functionality.

The OpenVPX Data Plane provides a Payload Slot Profile with a PCIe Fat Pipe (x4) up-to Gen 2 speeds, allowing high data throughput into, and out of the VF330.

The **VF330** Board Management supports Tier 1 IPMC functionality on the VPX Management Plane as per VITA 46.11. An onboard USB Debug interface for the FPGA simplifies development and system integration.

The **VF330** Rugged IO Processing card is used in airborne, maritime and land based systems, video and graphic processing, industrial control, low-power (SWaP) and many other applications. It seamlessly integrates with the VF360 and VF370 single board computer (SBC) processing cards from EC.

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SPECIFICATIONS

Typical Applications

- Rugged IO processing for airborne, maritime and land based systems
- Video and graphic processing, symbology overlay, etc.
- Industrial control
- Transport systems
- Low-power (SWaP) applications

Ordering Information (Generic Order Code = VF330-AB-C-DE)

A: FPGA Transceiver Speed (C, D)	C = 3.125 Gbps, D = 6.144 Gbps
B: FPGA Size (Logic Elements) (7, 9)	7 = 150K LEs, 9 = 300K LEs
C: FPGA DDR3 Size (0, 2)	None or 2 GB total DDR3 size (1 GB per bank)
D: Thermal (0, 1)	0 = air-cooled, 1 = conduction-cooled
E: Conformal Coating (0, 1)	0 = un-coated, 1 = conformal coated

The secondary video and IO interfaces on the high-density connector are accessed by means of an Adaptor Board that connects to the FM510 front panel.

On the Adaptor Board, two HD-BNC connectors provide a secondary video interface and two Samtec connectors provide twisted pair ribbon cable headers for IO connections (RS422, RS485, CAN, discrete IO and audio) to other sub-systems.

The secondary video interface on the Adaptor Board is configured in conjunction with the FM510 primary video configuration, e.g. the FM510–AD option has an analogue video input and SDI video output on the front panel, combined with a SDI video input and analogue video output on the Adaptor Board.

Block Diagram